Notice of Allowability	Application No.	Applicant(s)	
	10/706,972	YAMASHITA ET AL.	
	Examiner	Art Unit	
	Hien X. Vo	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amedment filed on 05/02/05*.

2. ☒ The allowed claim(s) is/are *1-29*.

3. ☒ The drawings filed on *14 November 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

Claims 1-29 allowed over the prior art record. Please see the previous office action and amendment filed on 05/02/05.

1. The following is an examiner's statement of reasons for allowance:

As per claims 1, none of the prior art teach singularly or in combination a semiconductor integrated circuit device which is built in the building structure including a sensor to detect a physical quantity related to the property of the building structure and a power circuit to apply power to the sensor; and an inspection device that receives a detect signal generated based upon the physical quantity detected by the semiconductor integrated circuit device and determines the quality of the building structure based upon the received detect signal, wherein the power circuit intermittently applies power to the sensor: and wherein the sensor detects the physical quantity when the power circuit applies power to the sensor.

As per claim 6, none of the prior art teach singularly or in combination a step for mounting a sensor in the building structure for generating a detect signal corresponding to a physical quantity related to a property of the building structure; a step for intermittently applying power to the sensor from a power circuit mounted on the semiconductor integrated circuit, a step for intermittently detecting the physical quantity related to the property of the building structure, when the power is applied to the sensor.

to generate the detect signal, a step for transmitting the detect signal to an inspection device provided outside the semiconductor integrated circuit device, and a step for determining the quality of the building structure based upon the detect signal received by the inspection device.

With respect to claims 14 and 22, none of the prior art teach singularly or in combination a sensor that detects physical quantity measurable by a semiconductor and related to the property of building structure, an A/D converter that amplifies a signal detected by the sensor and converts the signal to a digital signal, a microprocessor that processes the digital signal, a transmitter circuit that transmits a signal processed by the microprocessor to an external device, an electric power generator configured so that it supplies electric power to at least one of the sensor, the A/D converter, the microprocessor and the transmitter an electric power controller that controls whether electric power generated by the electric power generator is supplied to at least one of the sensor, the A/D converter, the microprocessor and the transmitter circuit or not; and a capacitor configured so that electric power generated by the electric power generator is stored.

With respect to claims 23 and 24, none of the prior art teach singularly or in combination a circuit device is buried and the quality of which can monitoring method for building structure, wherein semiconductor integrated be determined by a quality the quality monitoring method for building structure comprises steps of: a step for building a semiconductor integrated circuit device mounting a sensor for detecting physical quantity related to the property of the building structure and generating a detect signal

corresponding to the physical quantity in the building structure; a step for operating the sensor, detecting the physical quantity related to the property of the building structure and generating the detect signal corresponding to the physical quantity, a step for transmitting the detect signal to an inspection device provided outside the semiconductor integrated circuit device; and a step for determining the quality of the building structure based upon the detect signal received by the inspection device, an electric power controller configured so that it controls whether electric power generated by the electric power generator is supplied to at least one of the sensor, the A/D converter, the microprocessor and the transmitter circuit or not; and a capacitor configured so that it stores electric power generated by the electric power generator and a semiconductor integrated circuit device provided with a sensor for detecting physical quantity related to the property of the building structure is buried, and the quality can be determined based upon a detect signal corresponding to the physical quantity detected by the semiconductor integrated circuit device by the inspection device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hien X. Vo whose telephone number is (571) 272-2282. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hien Vo
05/12/05

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PRIM[illegible] EXAMINER

5/16/05